

## **LISTING OF CLAIMS**

- 1 1. (original) A content addressable memory (CAM) device comprising:  
2 a CAM array;  
3 a first counter circuit coupled to the CAM array, the first counter circuit being adapted to store an  
4 address value and to incrementally adjust the address value in response to a first control  
5 signal and to reset the address value to a start address in response to a second control signal;  
6 a second counter circuit to store a limit value and to incrementally adjust the limit value in response  
7 to the second control signal; and  
8 a compare circuit coupled to receive the address value from the first counter circuit and the limit  
9 value from the second counter circuit, the compare circuit being adapted to assert the second  
10 control signal if the address value and the limit value have a predetermined relationship.
- 1 2. (original) The CAM device of claim 1 wherein the compare circuit is adapted to compare the  
2 address value to the limit value and to assert the second control signal if the address value and the  
3 limit value are equal.
- 1 3. (previously presented) The CAM device of claim 1 wherein the second counter circuit is adapted to  
2 incrementally adjust the limit value in response to the second control signal after the second control  
3 signal has been delayed for a first delay time.
- 1 4. (previously presented) The CAM device of claim 1 wherein the first counter circuit is adapted to  
2 incrementally adjust the address value by increasing the address value by a predetermined amount.
- 1 5. (original) The CAM device of claim 4 wherein the predetermined amount is one.
- 1 6. (previously presented) The CAM device of claim 1 wherein the first counter circuit is adapted to  
2 incrementally adjust the address value by decreasing the address value by a predetermined amount.
- 1 7. (original) The CAM device of claim 1 wherein the start address corresponds to a highest priority

- 2 storage location in the CAM array.
- 1 8. (original) The CAM device of claim 1 wherein the start address is a lowest address that  
2 corresponds to a storage location within the CAM array.
- 1 9. (original) The CAM device of claim 1 wherein the start address is a highest address that  
2 corresponds to a storage location within the CAM array.
- 1 10. (original) The CAM device of claim 1 further comprising a programmable storage element to store  
2 the start address.
- 1 11. (original) The CAM device of claim 1 wherein the second counter circuit is responsive to a third  
2 signal to reset the limit value to an initial limit value.
- 1 12. (original) The CAM device of claim 11 wherein the initial limit value is an address value that  
2 corresponds to a highest priority storage location within the CAM array.
- 1 13. (original) The CAM device of claim 11 wherein the initial limit value is a lowest address that  
2 corresponds to a storage location within the CAM array.
- 1 14. (original) The CAM device of claim 11 wherein the initial limit value is a highest address that  
2 corresponds to a storage location within the CAM array.
- 1 15. (original) The CAM device of claim 11 further comprising a storage element to store the initial  
2 limit value.
- 1 16. (original) The CAM device of claim 15 wherein the storage element is programmable to store the  
2 initial limit value during operation of the CAM device.
- 1 17. (original) The CAM device of claim 1 wherein the second counter circuit is adapted to  
2 incrementally adjust the limit value by increasing the limit value by a predetermined amount.

1 18. (previously presented) The CAM device of claim 1 wherein the second counter circuit is adapted to  
2 incrementally adjust the limit value by decreasing the limit value by a predetermined amount.

1 19. (previously presented) The CAM device of claim 1 further comprising a third counter circuit to  
2 store a block select value, the third counter circuit being adapted to incrementally adjust the block  
3 select value in response to a third control signal and to assert the first control signal when the block  
4 select value reaches a predetermined value.

1 20. (original) The CAM device of claim 1 wherein the first counter circuit is adapted to detect when  
2 the limit value has reached a predetermined limit value and, in response, to generate a third control  
3 signal, the CAM device further comprising a third counter circuit to store a block select value, the  
4 third counter circuit being adapted to incrementally adjust the block select value in response to the  
5 third control signal.

1 21. (original) The CAM device of claim 20 wherein the third counter circuit is further adapted to reset  
2 the block select value to an initial block select value in response to a fourth control signal, and the  
3 CAM device further comprising:  
4 a fourth counter circuit to store a block select limit and to incrementally adjust the block select limit  
5 in response to the fourth control signal; and  
6 a block select compare circuit coupled to receive the block select value from the third counter  
7 circuit and the block select limit from the fourth counter circuit, the block select compare  
8 circuit being adapted to assert the fourth control signal if the block select value and the block  
9 select limit have a predetermined relationship.

1 22. (original) The CAM device of claim 1 wherein:  
2 the CAM array includes a plurality of rows of CAM cells and a plurality of word lines coupled  
3 respectively to the plurality of rows of CAM cells; and wherein the CAM device further  
4 comprises:

5 an address decoder coupled to the plurality of word lines and coupled to receive the address value  
6 from the first counter circuit, the address decoder being adapted to activate one of the  
7 plurality of word lines according to the address value such that a data word within the row of  
8 CAM cells coupled to the one of the plurality of word lines is output from the CAM array;  
9 and  
10 an error detector coupled to receive the data word from the CAM array and having circuitry to  
11 determine whether the data word contains an error.

1 23. (withdrawn) A method of operation within a content addressable memory (CAM) device, the  
2 method comprising:  
3 accessing data stored at a first address value in a CAM array;  
4 comparing the first address value with a second address value to determine if the first address value  
5 and the second address value have a predetermined relationship; and  
6 incrementally adjusting the second address value if the first address value and the second address  
7 value have the predetermined relationship.

1 24. (withdrawn) The method of claim 23 further comprising resetting the first address value to a start  
2 address if the first address value and the second address value have the predetermined relationship.

1 25. (withdrawn) The method of claim 24 wherein resetting the first address value to a start address  
2 comprises resetting the first address value to a start address that corresponds to a highest priority  
3 storage location in the CAM array.

1 26. (withdrawn) The method of claim 24 wherein resetting the first address value to a start address  
2 comprises resetting the first address value to a lowest address that corresponds to a storage location  
3 within the CAM array.

1 27. (withdrawn) The method of claim 24 wherein resetting the first address value to a start address  
2 comprises resetting the first address value to a highest address that corresponds to a storage location

3 within the CAM array.

1 28. (withdrawn) The method of claim 23 further comprising incrementally adjusting the first address  
2 value if the first address value and the second address value do not have the predetermined  
3 relationship.

1 29. (withdrawn) The method of claim 28 wherein incrementally adjusting the first address value  
2 comprises increasing the first address value by a predetermined amount.

1 30. (withdrawn) The method of claim 28 wherein incrementally adjusting the first address value  
2 comprises decreasing the first address value by a predetermined amount.

1 31. (withdrawn) The method of claim 23 wherein comparing the first address value with the second  
2 address value to determine if the first address value and the second address value have a  
3 predetermined relationship comprises determining if the first address value and the second address  
4 value are equal.

1 32. (withdrawn) The method of claim 23 wherein comparing the first address value with the second  
2 address value to determine if the first address value and second address value have a predetermined  
3 relationship comprises determining if the first address value is greater than the second address  
4 value.

1 33. (withdrawn) The method of claim 23 wherein incrementally adjusting the second address value  
2 comprises increasing the second address value by a predetermined amount.

1 34. (withdrawn) The method of claim 23 wherein incrementally adjusting the second address value  
2 comprises decreasing the second address value by a predetermined amount.

1 35. (withdrawn) The method of claim 23 further comprising:  
2 receiving a reset signal; and

- 3       resetting the second address value to an initial value.
- 1   36.   (withdrawn) The method of claim 35 wherein resetting the second address value to an initial value  
2       comprises resetting the second address value to an initial value that corresponds to a highest  
3       priority storage location in the CAM array.
- 1   37.   (withdrawn) The method of claim 35 wherein resetting the second address value to an initial value  
2       comprises resetting the second address value to a lowest address that corresponds to a storage  
3       location within the CAM array.
- 1   38.   (withdrawn) The method of claim 35 wherein resetting the second address value to an initial value  
2       comprises resetting the second address value to a highest address that corresponds to a storage  
3       location within the CAM array.
- 1   39.   (original) A content addressable memory (CAM) device comprising:  
2       means for accessing data stored at a first address value in a CAM array;  
3       means for comparing the first address value with a second address value to determine if the first  
4           address value and the second address value have a predetermined relationship; and  
5       means for incrementally adjusting the second address value if the first address value and the second  
6       address value have the predetermined relationship.
- 1   40.   (original) The CAM device of claim 39 further comprising means for resetting the first address  
2       value to a start address if the first address value and the second address value have the  
3       predetermined relationship.
- 1   41.   (original) The CAM device of claim 39 further comprising means for incrementally adjusting the  
2       first address value if the first address value and the second address value do not have the  
3       predetermined relationship.
- 1   42.   (original) The CAM device of claim 41 wherein the means for incrementally adjusting the first

2 address value comprises means for increasing the first address value by a predetermined amount.

1 43. (original) The CAM device of claim 41 wherein the means for incrementally adjusting the first  
2 address value comprises means for decreasing the first address value by a predetermined amount.

1 44. (previously presented) A content addressable memory (CAM) device comprising:  
2 a CAM array having a plurality of rows of CAM cells;  
3 a first counter to store an address for one of the rows of CAM cells;  
4 a second counter to store a limit value;  
5 a compare circuit coupled to the first and second counters to compare the address with the limit  
6 value; and  
7 an address decoder coupled to the first counter and the CAM array to select one of the rows of  
8 CAM cells corresponding to the address.

1 45. (original) The CAM device of claim 44 further comprising an error detector coupled to the CAM  
2 array to receive a data word from the selected one the rows of CAM cells and to detect whether  
3 there is an error in the data word.

1 46. (original) The CAM device of claim 44 wherein the CAM array comprises a plurality of CAM  
2 array blocks, and wherein the CAM device further comprises a third counter coupled to the first  
3 counter, the third counter to store a block select value to select one of the CAM array blocks.

1 47. (original) The CAM device of claim 46 wherein the third counter is coupled to receive the address  
2 from the first counter.

1 48. (original) The CAM device of claim 46 wherein the first counter is coupled to receive the block  
2 select value from the third counter.

1 49. (previously presented) The CAM device of claim 46 further comprising:  
2 a fourth counter to store a block select limit; and

3 a second compare circuit coupled to the third and fourth counters to compare the block select value  
4 and the block select limit.

1 50. (withdrawn) A content addressable memory (CAM) device comprising:  
2 a CAM array having a plurality of rows of CAM cells; and  
3 address circuitry coupled to the plurality of rows of CAM cells and adapted to access the rows in a  
4 biased sequence order.

1 51. (withdrawn) The CAM device of claim 50 further comprising an error detector coupled to the  
2 CAM array to receive data from the accessed rows and detect whether there is an error in the data.

1 52. (withdrawn) The CAM device of claim 50 wherein the address circuitry comprises:  
2 a first counter;  
3 a second counter;  
4 a compare circuit coupled to outputs of the first and second counters; and  
5 an address decoder coupled to the first counter and the rows of CAM cells.

1 53. (withdrawn) The CAM device of claim 50 wherein the CAM array includes a plurality of CAM  
2 array blocks each including a plurality of rows of CAM cells that is a subset of the plurality of rows  
3 of CAM cells in the CAM array, and wherein the address circuitry is adapted to access the rows  
4 included within each of the CAM array blocks in a biased sequence order.

1 54. (withdrawn) The CAM device of claim 53 wherein the address circuitry is further adapted to  
2 access the blocks in a linear sequence order.

1 55. (withdrawn) The CAM device of claim 53 wherein the address circuitry is further adapted to  
2 access the blocks in a biased sequence order.

1 56. (withdrawn) The CAM device of claim 53 wherein the address circuitry comprises:  
2 a first counter;



3 a second counter;  
4 a first compare circuit coupled to outputs of the first and second counters;  
5 an address decoder coupled to the first counter and the rows of the CAM array blocks; and  
6 a third counter coupled to the first counter.

1 57. (withdrawn) The CAM device of claim 56 further comprises:  
2 a fourth counter; and  
3 a second compare circuit coupled to outputs of the third and fourth counters.

1 58. (withdrawn) A method of operation within a content addressable memory (CAM) device, the  
2 method comprising:  
3 accessing rows of CAM cells in a CAM array in a biased sequence order; and  
4 detecting whether data stored in each accessed row contains an error.

1 59. (withdrawn) The method of claim 58 wherein the CAM array includes a plurality of CAM array  
2 blocks, and the method further comprises accessing rows of CAM cells in a first one of the CAM  
3 array blocks in a biased sequence order.

1 60. (withdrawn) The method of claim 59 further comprising selecting the CAM array blocks in a linear  
2 sequence order.

1 61. (withdrawn) The method of claim 59 further comprising selecting the CAM array blocks in a  
2 biased sequence order.